Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) A memory device as claimed in claim 21, wherein the piezoelectric material is a ferroelectric material.

3-5. (Canceled)

6. (Currently Amended) A memory device as claimed in ~~claim 2,~~ claim 21, ~~wherein the respective~~ the plurality of first electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a first plane,

the ~~respective~~ plurality of second electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a second plane, and

the ~~respective~~plurality of third electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a third plane,

~~with the planes~~the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of third electrodes being ~~parallel with each other and the second electrodes being~~ perpendicular to the ~~first and third~~plurality of second electrodes.

7-16. (Canceled)

17. (Currently Amended) A memory device as claimed in ~~claim 3,~~claim 24, ~~wherein the respective~~the plurality of first electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of ~~respective~~ second electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a second plane, and

the ~~respective~~plurality of third electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a third plane,

~~with the planes~~the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes ~~being parallel with each other and the second electrodes~~ being perpendicular to the plurality of second~~first and third~~ electrodes.

18. (Currently Amended) A memory device as claimed in ~~claim 4,~~claim 25,

~~-~~the plurality of ~~wherein the respective~~ first electrodes being~~are~~ arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of ~~the respective~~ second electrodes being~~are~~ arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of ~~the respective~~ third electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a third plane, ~~with the planes~~

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of ~~the~~ first and the plurality of third electrodes being ~~parallel with each other and the second electrodes being~~ perpendicular to the ~~first and third~~plurality of second electrodes.

19. (Currently Amended) A memory device as claimed in ~~claim 21,~~claim 26,

~~-wherein the respective~~the plurality of first electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of ~~respective~~ second electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a second plane, and

the ~~respective~~plurality of third electrodes ~~are~~being arranged parallel to each other in a spaced apart manner in a third plane,

~~with the planes~~the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes ~~being parallel with each other and the second electrodes~~ being perpendicular to the plurality of second~~first and third~~ electrodes.

20. (Canceled)

21. (Currently Amended) A memory device comprising:

a plurality of first electrodes;

a plurality of second electrodes;

a plurality of third electrodes;

a two-dimensional array of memory cells provided corresponding to intersections between the plurality of first electrodes and the plurality of second electrodes and to intersections between the plurality of second electrodes and the plurality of third electrodes; and

~~a plurality of memory cells provided corresponding to intersections between the plurality of first electrodes and the plurality of second electrodes; and~~

a plurality of comparators, one for each row of the memory cells, each of the comparators~~which has~~ having a first input and a second input,

each of the plurality of memory cells including a first layer including a piezoelectric material and a second layer including a ferroelectric material,

one second electrode of the plurality of the second electrodes being provided between the first layer and the second layer,

the first layer and the second layer being provided between one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes,

the one first electrode being connected to the first input of one of the plurality of comparators and the one third electrode being connected to the second input of the same one ~~included in one comparator~~ of the plurality of comparators~~, and~~

~~the one third electrode being connected to the second input included in the one comparator~~.

22. (Currently Amended) A memory device as claimed in claim 21, ~~wherein~~ ~~said~~the one comparator ~~compares~~comparing a first ~~signal~~voltage between the one first electrode and the one second electrode with a second ~~signal~~voltage between the one third electrode and the one second electrode.

23. (New) A memory device as claimed in claim 22,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of third electrodes being perpendicular to the plurality of second electrodes.

24. (New) A memory device comprising:

a plurality of first electrodes;

a plurality of second electrodes;

a plurality of third electrodes;

a plurality of memory cells provided corresponding to intersections between the plurality of first electrodes and the plurality of second electrodes and to intersections between the plurality of second electrodes and the plurality of third electrodes; and

a plurality of comparators that are provided corresponding to a plurality of pairs of the plurality of first electrodes and the plurality of third electrodes;

each of the plurality of memory cells including a first layer including a piezoelectric material and a second layer including a ferroelectric material,

one second electrode of the plurality of the second electrodes being provided between the first layer and the second layer, and

the first layer and the second layer being provided between one first electrode of the plurality of first electrodes and one third electrode of the plurality of third electrodes.

25. (New) The memory device as claimed in claim 24,

one memory cell of the plurality of memory cells being provided between the one first electrode and the third electrode.

26. (New) The memory device as claimed in claim 24,

each of the plurality of comparators being arranged for one of the plurality of pairs of the plurality of first electrodes and the plurality of their electrodes.

27. (New) The memory device as claimed in claim 24,

each of the plurality of comparators having a first input that is coupled to one first electrode of one pair of the plurality of first electrodes and the plurality of third electrodes and a second input that is coupled to the one third electrode of the one pair.

28. (New) The memory device as claimed in claim 27,

one of the plurality of comparators comparing a first voltage between the one first electrode and the one second electrode with a second voltage between the one third electrode and the one second electrode.

29. (New) The memory device as claimed in claim 27,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.

30. (New) The memory device as claimed in claim 28,

the plurality of first electrodes being arranged parallel to each other in a spaced apart manner in a first plane,

the plurality of second electrodes being arranged parallel to each other in a spaced apart manner in a second plane, and

the plurality of third electrodes being arranged parallel to each other in a spaced apart manner in a third plane,

the first plane, the second plane and the third plane being parallel to each other, and

the plurality of first electrodes and the plurality of the third electrodes being perpendicular to the plurality of second electrodes.